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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **Edward B. Stokes**

Application No.: **10/693,126** Examiner: **Junghwa M. IM**

Filed: **October 24, 2003** Docket No.: **GLOZ 200170**

For: **FLIP-CHIP LIGHT EMITTING DIODE**

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Applicant(s) transmit(s) herewith one (1) originally signed copy of the APPEAL BRIEF UNDER 37 C.F.R. § 41.37 for the above-identified patent application.

Applicant(s) respectfully requests a one-month extension of time up to and including at least March 23, 2006, to submit this Appeal Brief.

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Respectfully submitted,
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March 23, 2006
Date

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re the Application of

Edward B. STOKES

Application No.: 10/693,126 Examiner: Junghwa M. IM

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For: FLIP-CHIP LIGHT EMITTING DIODE

BRIEF ON APPEAL

Appeal from Group 2811

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I. REAL PARTY IN INTEREST

The real party in interest for this appeal and the present application is GELcore LLC, by way of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 014978, Frame 0370.

II. STATEMENT OF RELATED APPEALS AND INTERFERENCES

There are no prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 2-13, 16, 17, 29, and 30 are on appeal.

Claims 2-18, 29, and 30 are pending.

Claims 14, 15, and 18 are allowed.

Claims 2-13, 16, 17, 29, and 30 are rejected.

Claims 1 and 19-28 are canceled.

IV. STATUS OF AMENDMENTS

A Response to Final Office Action was filed on December 21, 2005. This Response listed the currently pending claims and included remarks, but did not include any amendments to the claims. An Advisory Action was mailed January 23, 2006 responsive to the Response to Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention of independent **claim 3** is directed to a flip chip light emitting diode die (10, 10', 10"). A plurality of semiconductor layers (14, 14', 14") are disposed on a light-transmissive substrate (12, 12', 12"). The semiconductor layers include a p-type layer (24, 24', 24") and an n-type layer (20, 20', 20"). The semiconductor layers define a device mesa (30, 30', 30"). A reflective electrode (34, 34', 34") is disposed on the device mesa to energize the device mesa to produce light and to reflect the light produced by the device mesa toward at least one of the light-transmissive substrate and sides of the device mesa (at least at page 7 lines 20-23). The reflective electrode includes electrical connecting material (44, 44', 44", 62) disposed over portions of the device mesa and making electrical contact with the device mesa, and a light transmissive dielectric layer (42, 42', 60, 80) laterally interspersed with the electrical connecting material. The reflective electrode has laterally periodic reflectivity modulations (at least at page 9 lines 23-24).

The invention of dependent **claim 12** includes all recited elements of claim 3. Additionally, the interspersing of the electrical connecting material (44, 44', 44", 62) and the dielectric layer (42, 42', 60, 80) define a reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa (at least at page 9 lines 23-29).

The invention of independent **claim 29** is also directed toward a flip chip light emitting diode die (10, 10', 10"). A plurality of semiconductor layers (14, 14', 14") are disposed on a light-transmissive substrate (12, 12', 12"). The semiconductor layers include a p-type layer (24, 24', 24") and an n-type layer (20, 20', 20"). The semiconductor layers define a device mesa (30, 30', 30"). A reflective electrode (34,

34', 34") is disposed on the device mesa to energize the device mesa to produce light and to reflect the light produced by the device mesa toward at least one of the light-transmissive substrate and sides of the device mesa (at least at page 7 lines 20-23). The reflective electrode includes electrical connecting material portions (44, 44', 44", 62) disposed over the device mesa and making electrical contact with the device mesa, and light transmissive dielectric portions (42, 42', 60, 80) disposed over the device mesa and laterally interspersed with the electrical connecting material portions.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

- Whether **claim 3** is properly rejected under 35 U.S.C. §103(a) as being unpatentable over Camras et al., U.S. Patent No. 6,784,463 (hereinafter "Camras") in view of Sawayama et al., U.S. Patent No. 6,788,366 (hereinafter "Sawayama") (Addressed in Argument VII-A);
- Whether **claim 12** is properly rejected under 35 U.S.C. §103(a) as being unpatentable over Camras in view of Sawayama (Addressed in Argument VII-B); and
- Whether **claim 29** is properly rejected under 35 U.S.C. §103(a) as being unpatentable over Camras in view of Sawayama (Addressed in Argument VII-C).

VII. ARGUMENT

A. Claim 3 patentably distinguishes over the combination of Camras and Sawayama.

Fig. 3A of the Camras reference is reproduced below:

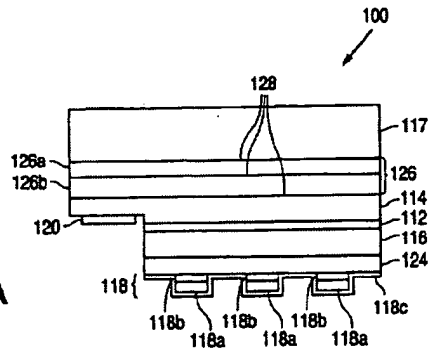


FIG. 3A

where element (117) is a light-transmissive superstrate (Camras col. 4 lines 42, 64-65), the layers (114, 112, 116) define a pn diode structure (Camras col. 4 lines 25-41), layer (124) generically represents additional structure such as a semiconductor spreading layer or a metal layer (Camras col. 7 lines 8-24), and the structure (118) is a reflective contact including ohmic contacts (118a) disposed on a patterned semiconductor layer (118b), and layer (118c) is a reflective metal layer of gold, aluminum, or silver (Camras col. 6 lines 53-60). The proposed combination of Camras and Sawayama equates the electrical connecting material of claim 3 with the ohmic contacts (118a) of Camras, and recognizes that Camras does not disclose a light transmissive dielectric layer laterally interspersed with the electrical connecting material, as called for in claim 3. (Final Office Action mailed Sept. 22, 2005 at pages 2-3).

The proposed combination looks to Fig. 4 of Sawayama as disclosing a light transmissive dielectric layer (5c) which is laterally interspersed with electrical connecting material (7). Appellants understand this proposed combination as modifying Camras by interspersing the dielectric material (5c) of Sawayama between the ohmic

contact regions (118a) of Camras (or, equivalently, by replacing the ohmic contact regions (118a) and lateral gaps therebetween with the structure (5c,7) of Sawayama), with the reflective layer (118c) then disposed over both the ohmic contact regions (118a) and the added dielectric regions (5c).

As an initial matter, claim 3 calls for the reflective electrode to have laterally periodic reflectivity modulations. In the proposed combination of Camras and Sawayama, this feature is alleged to be disclosed in Camras "through having a waveform of reflectivity in terms of time." (Final Office Action at page 2). Claim 3 calls for laterally periodic reflectivity modulations, not temporal reflectivity modulations. Elsewhere, the Office Action states that the electrode has laterally periodic modulation. (Office Action at page 3).

The layer (118b) is referred to in Camras as a "patterned semiconductor layer" (Camras col. 6 line 57). The patterned semiconductor layer (118b) appears to be drawn with a periodic regularity in Camras Fig. 3a; however, this is nowhere stated in the text of Camras, which instead says: "The geometry of the pattern of semiconductor layer 118b (and hence of ohmic contacts 118a) depends upon the requirements for current spreading and optical transparency. Since the material in patterned semiconductor layer 118b may absorb light emitted by active region 112, layer 118b should be thin and the surface area of layer 124 covered by layer 118b should be relatively small." (Camras col. 7 lines 1-7).

Regarding the use of drawings as prior art, MPEP § 2125 states that: "When the reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value. However, the description of the article pictured can be relied on, in combination

with the drawings, for what they would reasonably teach one of ordinary skill in the art." MPEP § 2125 (internal citations omitted). Camras expressly states that the drawings are not necessarily to scale. (Camras col. 4 lines 4-5). Accordingly, it does not appear that Camras discloses or fairly suggests a reflective electrode having laterally periodic reflectivity modulations.

Appellants further respectfully submit that there is no motivation to make the proposed combination of Camras and Sawayama.

The motivation proposed for such a combination is "to incorporate the teachings of Sawayama into the device of Camras in order to have a light-transmissive dielectric layer laterally interspersed with the electrical connecting material to protect the reflective electrode." (Final Office Action mailed Sept. 22, 2005 at page 3). Responsive to Appellants' traversal of this motivation in the Response to Final Office Action filed on December 21, 2005, the Advisory Action further states that "the dielectric layer 5c protects/supports the bottom portion of the reflective electrode layer. In addition, it is pointed out that the dielectric layer formation between the connection electrode portion [7's] is substantially identical to the one in the instant invention. That is, the instant invention also shows that a dielectric layer [42] is formed between connecting, conductive layers [44's]." (Advisory Action mailed Jan. 23, 2006).

However, the reflective contact (118) of Camras is fully supported in its existing design shown in Camras Fig. 3a. The ohmic contact material (118a) is fully supported by the patterned semiconductor layer (118b), and the reflective metal layer (118c) is fully supported by the ohmic contact material (118a) and intervening regions of the layer (124). The skilled artisan would not be motivated to complicate the design of the LED of Camras Fig. 3a by introducing additional dielectric regions (5c) to provide redundant

support for the already fully supported reflective contact (118). Thus, a support-based motivation is untenable. As far as providing protection for the bottom portion of the electrode, this proposed motivation apparently refers to the reflective metal layer (118c), as the proposed interspersed dielectric (5c) would contact only the bottom of the reflective metal layer (118c). It is not clear what sort of bottom protection is needed for the reflective metal layer (118c). It is disposed on layer (124) which is an epitaxial semiconductor layer or a deposited metal layer, both of which are typically quite smooth and capable of protecting the reflective metal layer (118c).

As neither the support-based proposed motivation nor the protection-based proposed motivation is tenable, it is respectfully submitted that no prima facie case has been made for the proposed combination of Camras and Sawayama. Accordingly, Appellants respectfully request reversal of the rejection of claim 3 based on the combination of Camras and Sawayama.

B. Claim 12 patentably distinguishes over the combination of Camras and Sawayama.

Claim 12 calls for the interspersing of the electrical connecting material and the dielectric layer to define a reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa.

The explanation for rejection of claim 12 is as follows:

> Regarding claim 12, the combined teachings of Camras and Sawayama does not explicitly show that "the interspersing of the electrical connecting material and the dielectric layer define a reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa." However, it is obvious that the device with the combined teachings of Camras and Sawayama has the characteristics in which the interspersing of the electrical connecting material and the dielectric layer define a

> reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa since the waveform of the reflectivity is realized by the interspersing of the electrical connecting material and the dielectric layer.

Final Office Action at pages 4-5.

A diffraction grating has a periodicity selected to provide the desired diffraction of a selected wavelength. As discussed previously, Camras does not appear to disclose or fairly suggest a reflective electrode having laterally periodic reflectivity modulations.

However, even if the apparent regularity in Fig. 3a of the patterned semiconductor layer (118b) is taken as disclosure of a reflective electrode having laterally periodic reflectivity modulations, it does not follow that this alleged periodicity defines a reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa. Such optimization involves providing at least a period of the periodicity selected to provide desired diffraction of the characteristic wavelength of the light produced by the device mesa. There is no disclosure or fair suggestion in Camras to provide such a period designed to produce desired diffraction of the characteristic wavelength of the light produced by the device mesa.

Accordingly, Appellants respectfully submit that the proposed combination of Camras and Sawayama does not disclose or fairly suggest the limitation of claim 12 that the interspersing of the electrical connecting material and the dielectric layer define a reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa. Accordingly, Appellants respectfully request reversal of the rejection of claim 12 based on the combination of Camras and Sawayama.

C. Claim 29 patentably distinguishes over the combination of Camras and Sawayama.

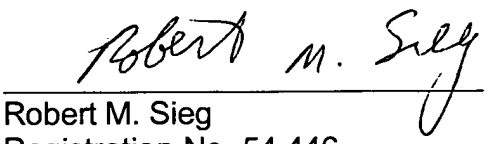
Claim 29 differs from claim 3 at least in that claim 29 omits the limitation that the reflective electrode have laterally periodic reflectivity modulations.

The rejection of claim 29 again employs the proposed combination of Camras and Sawayama. The Final Office Action again proposes as motivation to combine "to incorporate the teachings of Sawayama into the device of Camras in order to have a light-transmissive dielectric layer laterally interspersed with the electrical connecting material to protect the reflective electrode." (Final Office Action mailed Sept. 22, 2005 at page 6). Appellants' traversal of this proposed motivation to combine set forth herein respective to claim 3 applies equally well to the rejection of claim 29, and Appellants therefore respectfully request reversal of the rejection of claim 29 based on the combination of Camras and Sawayama.

VIII. CONCLUSION

For all of the reasons discussed above, it is respectfully submitted that the rejections are in error and that appealed claims 2-13, 16, 17, 29, and 30 are in condition for allowance. For all of the above reasons, Appellants respectfully request this Honorable Board to reverse the rejections of claims 2-13, 16, 17, 29, and 30.

Respectfully submitted,



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CLAIMS APPENDIX

CLAIMS INVOLVED IN THE APPEAL:

2. The flip chip light emitting diode die as set forth in claim 3, wherein the periodic reflectivity modulations define a diffraction grating that provides a predetermined diffraction of the light produced by the device mesa.

3. A flip chip light emitting diode die including:

a light-transmissive substrate;

a plurality of semiconductor layers disposed on the light-transmissive substrate, the semiconductor layers including a p-type layer and an n-type layer, the semiconductor layers defining a device mesa; and

a reflective electrode disposed on the device mesa to energize the device mesa to produce light and to reflect the light produced by the device mesa toward at least one of the light-transmissive substrate and sides of the device mesa, the reflective electrode including electrical connecting material disposed over portions of the device mesa and making electrical contact with the device mesa and a light-transmissive dielectric layer laterally interspersed with the electrical connecting material, the reflective electrode having laterally periodic reflectivity modulations.

4. The flip chip light emitting diode die as set forth in claim 3, wherein the electrical connecting material defines isolated regions, and the reflective electrode further includes:

an electrically conductive reflective layer disposed over the dielectric layer and the electrical connecting material, the reflective layer laterally electrical interconnecting the isolated regions of the electrical connecting material.

5. The flip chip light emitting diode die as set forth in claim **4**, wherein the reflective electrode further includes:

a electrically conductive bondable layer disposed on the electrically conductive reflective layer.

6. The flip chip light emitting diode die as set forth in claim **4**, wherein the reflective electrode further includes:

a current-spreading layer disposed between the device mesa and the dielectric layer.

7. The flip chip light emitting diode die as set forth in claim **6**, wherein the current-spreading layer includes:

a light-transmissive electrically conductive layer.

8. The flip chip light emitting diode die as set forth in claim **7**, wherein the light-transmissive electrically conductive layer includes:

a thin film of a light-absorbing material, the thin film having a thickness of less than about 10 nm and greater than 70% light transmission.

9. The flip chip light emitting diode die as set forth in claim **8**, wherein the light-absorbing material is selected from a group consisting of nickel oxide, gold, indium tin oxide, and zinc oxide.

10. The flip chip light emitting diode die as set forth in claim **7**, wherein the current-spreading layer includes:

a topmost one or more of the plurality of semiconductor layers.

11. The flip chip light emitting diode die as set forth in claim **4**, wherein the dielectric layer has a thickness selected to define an interference reflector optimized for a characteristic wavelength of the light produced by the device mesa.

12. The flip chip light emitting diode die as set forth in claim **3**, wherein the interspersing of the electrical connecting material and the dielectric layer define a reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa.

13. The flip chip light emitting diode die as set forth in claim **3**, wherein the dielectric layer is selected from a group consisting of a silicon oxide (SiO_x), a silicon nitride (SiN_x), and a silicon oxynitride (SiO_xN_y), where x and y correspond to stoichiometric parameters.

16. The flip chip light emitting diode die as set forth in claim **3**, wherein an interface disposed between the plurality of semiconductor layers and the reflective

electrode is roughened to scatter the reflected light toward the sides of the device mesa.

17. The flip chip light emitting diode die as set forth in claim **16**, wherein roughening includes a lateral periodicity defining a diffraction grating.

29. A flip chip light emitting diode die including:

a light-transmissive substrate;

a plurality of semiconductor layers disposed on the light-transmissive substrate, the semiconductor layers including a p-type layer and an n-type layer, the semiconductor layers defining a device mesa; and

a reflective electrode disposed on the device mesa to energize the device mesa to produce light and to reflect the light produced by the device mesa toward at least one of the light-transmissive substrate and sides of the device mesa, the reflective electrode including electrical connecting material portions disposed over the device mesa and making electrical contact with the device mesa and light-transmissive dielectric portions disposed over the device mesa and laterally interspersed with the electrical connecting material portions.

30. The flip chip light emitting diode die as set forth in claim **29**, wherein the electrical connecting material portions are isolated from one another, and the reflective electrode further includes:

an electrically conductive reflective layer disposed over the connecting material portions and the dielectric portions, the reflective layer laterally electrical interconnecting the isolated electrical connecting material portions.

EVIDENCE APPENDIX

A copy of each of the following items of evidence relied on by the Examiner is attached:

Camras et al., U.S. Patent No. 6,784,463; and

Sawayama et al., U.S. Patent No. 6,788,366.

Both these items of evidence were entered into the record by the Examiner in the Office Action mailed March 28, 2005.

RELATED PROCEEDINGS APPENDIX

NONE